

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/737,416	12/15/2003	Hakan Oner	021803-4.00US	6359	
20350 7	7590 06/29/2005		EXAMINER		
	AND TOWNSEND	CHO, JAMES HYONCHOL			
TWO EMBAR EIGHTH FLO	CADERO CENTER OR		ART UNIT	PAPER NUMBER	
SAN FRANCI	FRANCISCO, CA 94111-3834		2819		
			DATE MAILED: 06/29/2003	5	

Please find below and/or attached an Office communication concerning this application or proceeding.

			4.
	Application No.	Applicant(s)	
	10/737,416	ONER ET AL.	
Office Action Summary			
	James Cho	2819	
The MAILING DATE of this communication ap			5
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a replevent of the period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statuth Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a sly within the statutory minimum of th will apply and will expire SIX (6) MC e, cause the application to become A	reply be timely filed irty (30) days will be considered timely. NTHS from the mailing date of this commun	lication.
Status			
1) Responsive to communication(s) filed on 15 L	December 2003.		
· ·	s action is non-final.		
3) Since this application is in condition for allowa	ance except for formal ma	tters, prosecution as to the mer	its is
closed in accordance with the practice under	Ex parte Quayle, 1935 C.	D. 11, 453 O.G. 213.	
Disposition of Claims			
4)⊠ Claim(s) <u>1-31</u> is/are pending in the application	٦.		
4a) Of the above claim(s) is/are withdra	awn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>1-4 and 27-30</u> is/are rejected.			
7)⊠ Claim(s) <u>5-26 and 31</u> is/are objected to.			
8) Claim(s) are subject to restriction and/o	or election requirement.		
Application Papers		•	
9)☐ The specification is objected to by the Examin	er.		
10) The drawing(s) filed on is/are: a) acc	cepted or b) objected to	by the Examiner.	
Applicant may not request that any objection to the	e drawing(s) be held in abeya	ance. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including the correct	ction is required if the drawin	g(s) is objected to. See 37 CFR 1.	121(d).
11)☐ The oath or declaration is objected to by the E	xaminer. Note the attache	ed Office Action or form PTO-15	52.
Priority under 35 U.S.C. § 119			
12) ☐ Acknowledgment is made of a claim for foreign a) ☐ All b) ☐ Some * c) ☐ None of: 1. ☐ Certified copies of the priority documen	ts have been received.		
2. Certified copies of the priority documen		· ·	
3. Copies of the certified copies of the price	-	n received in this National Stag	е
application from the International Burea	` ' ' '	t ranaiwad	
* See the attached detailed Office action for a list	t of the certified copies no	t received.	
Attachment(s)			
1) M Notice of References Cited (PTO-892)	4) \prod Interview	Summary (PTO-413)	
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No	(s)/Mail Date	
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)) 5)	Informal Patent Application (PTO-152)	t in
Paper No(s)/Mail Date	6) 🗀 Other:	·	

Application/Control Number: 10/737,416

Art Unit: 2819

DETAILED ACTION

Claim Objections

Claim 27 is objected to because of the following informalities:

"second terminals" on line 2 and 5 appears to be --second output terminals-respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 4 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi (US PAT No. 6,356,141).

Regarding claim 1, Fig. 1 of Yamauchi teaches a low-voltage differential signal driver having first and second output terminals (Vo1, Vo2), the low-voltage differential signal driver comprising: a current sourcing circuit (11) adapted to generate a current (Idp); a current steering circuit (12,13,15,16) coupled to receive the generated current and first and second input signals, where in response to the first and second input signals the current steering circuit steers the current either in a first direction (IN being low and XIN being high; col. 3, lines 60-67) to generate a positive differential voltage across the first and second output terminals or in a second direction (IN being high and

Art Unit: 2819

XIN being low; col. 3, line 67 - col. 4, line 6) to generate a negative differential voltage across the first and second output terminals; a current sinking circuit (14) coupled to the current steering circuit and adapted to receive and sink the generated current; a voltage dividing circuit (Rt, Rt) disposed between the first and second output terminals (Vo1, Vo2) and adapted to divide the voltage generated between the first and second output terminals; a first voltage regulating circuit (40) coupled to the current sinking circuit (14) and the current steering circuit (via 122 and 124); and a second voltage regulating circuit (35) coupled to the current sourcing circuit (11) and the voltage dividing circuit (Rt).

Regarding claim 2, Fig. 1 of Yamauchi teaches the low-voltage differential signal driver of claim 1, where the first voltage regulating circuit further comprises a first differential amplifier (35), and where the second voltage regulating circuit further comprises a second differential amplifier (40).

Regarding claim 3, Fig. 1 of Yamauchi teaches the low-voltage differential signal driver of claim 2 further comprising a replicating circuit (36, 37, 38) adapted to receive a first voltage supply (Vdd) and deliver a reference voltage signal (voltage at Nn) to the first voltage regulating circuit (to positive terminal of 40).

Art Unit: 2819

Regarding claim 4, Fig. 1 of Yamauchi teaches the low-voltage differential signal driver of claim 3 where the first voltage supply (Vdd) supplies its voltage to the second voltage regulating circuit (to positive terminal of 35)..

Regarding claim 27, Fig. 1 of Yamauchi teaches method for supplying a low-voltage differential signal across first and second terminals (Vo1, Vo2), the method comprising: generating a current (11, Idp) using a first voltage (Vgp); steering the generated current in a first direction to generate a positive differential output voltage across the first and second terminals in response to a first set of input signals (IN being low and XIN being high; col. 3, lines 60-67) and steering the generated current in a second direction to generate a negative differential output voltage across the first and second terminals in response to a second set of input signals (IN being high and XIN being low; col. 3, line 67 - col. 4, line 6); dividing the differential output voltage generated between the first and second input terminals to generate a weighted average thereof (Vm); regulating the weighted average of the differential output voltage (col. 4, lines 19-24); sinking the generated current (14, Idn); and regulating the first voltage (30).

Regarding claim 28, Fig. 1 of Yamauchi teaches the method of claim 27 where the weighted average of the differential output voltage is regulated using an operational amplifier (35) that receives a first supply voltage (voltage at Np) at one of its input terminals (positive terminal of 35).

Regarding claim 29, Fig. 1 of Yamauchi teaches the method of claim 28 where the first voltage is regulated using a reference voltage generated by a replicating circuit (col. 4, lines 25-40).

Regarding claim 30, Fig. 1 of Yamauchi teaches the method of claim 29 further comprising: limiting the current flowing out of or into the first and second output terminals (col. 4, lines 16-24).

Allowable Subject Matter

Claims 5-26 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Yamauchi teaches a driver with a constant current output, one of ordinary skill in the art would not have been motivated to modify the teaching of Yamauchi to further includes, among other things, the specific of the replicating circuit further comprising a third voltage regulating circuit as required by claim 5, and the method of tri-stating the differential output voltage as required by claim 31.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2819

Roper et al. (US PAT No. 6,900,663) discloses a low voltage differential signal driver circuit.

Preuss et al. (US PAT No. 6,603,348) discloses a center tap level control for current mode differential driver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho Primary Examiner Art Unit 2819

6-27-2005